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[STRUCTURE AND METHOD FOR LOCAL RESISTOR ELEMENT IN INTEGRATED CIRCUIT TECHNOLOGY]

Abstract

A method and system for forming a semiconductor device having superior ESD protection characteristics. A resistive material layer is disposed within a contact hole on at least one of the contact stud upper and lower surface. In preferred embodiments, the integral resistor has a resistance value of between about one Ohm and about ten Ohms, or between 10 and 100 Ohms. Embodiments of the resistive layer include sputtered silicon material, a tunnel oxide, a tunnel nitride, a silicon-implanted oxide, a silicon-implanted nitride, or an amorphous polysilicon. Embodiments of the invention include SRAMs, bipolar transistors, SOI lateral diodes, MOSFETs and SiGe Transistors.